Analysis of Synchronization Techniques in Grid Connected Photovoltaic System

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Abstract:

Maximum Power Point Tracking (MPPT), Grid synchronization, Islanding, DC-link voltage control and Current control are the major factors which are required for a grid-tied photovoltaic system to work efficiently and effectively. Phase, amplitude and frequency of the utility voltage are critical information for the operation of the grid-connected inverter system. Grid synchronization schemes provides phase, amplitude and frequency of utility voltage which is used to generate reference signal. Actuate and fast detection of these parameters are essential in order to keep grid parameters within range as mentioned in standards. This paper analyze different grid synchronization schemes used in grid connected photovoltaic system. The algorithms were initially analyzed in Matlab Simulink and validated in hardware.

1 INTRODUCTION:

In the present scenario of world energy sector, renewable sources are growing their importance day by day. This is mainly because of limited resource and bad environmental impacts of the conventional energy. Among the all renewable energy resources available, solar energy seems to be a major competitor as it is abundant in nature and its conversion to electricity through photovoltaic (PV) process is pollution-free. Increasing interest in PV systems, demands growth in research and development activities in various aspects such as Maximum Power Point Tracking (MPPT), PV arrays, anti-islanding protection, stability and reliability, power quality and power electronic interface.

A Microgrid consists of multiple distributed generators (DGs), renewable energy sources, conventional energy generators and energy storage systems those which provide both electric power and thermal energy as shown in figure.1. Typically, a Microgrid operates in parallel with the main grid. Microgrid may be operating in an islanded mode or in a standalone state. Islanded distributed generators (DGs) in a microgrid can change its operational mode to grid connected operation by synchronization with the main grid i.e. reconnection to the grid. A Microgrid or a portion of the power grid can be isolated from grid. However, the synchronization of microgrids that operate with multiple distributed generators (DGs) and loads cannot be controlled by a traditional synchronizer. It is necessary to control multiple distributed generators and energy storage systems in a coordinated way for the microgrid synchronization. Power converter system can be operated in islanded or standalone mode. In ideal condition, the output voltage parameters like amplitude, frequency and phase cannot be controlled for a grid together where multiple DGs are working in parallel; whereas the same parameters for standalone inverter to be connected to grid can be controlled by means of the various control strategies.

The Inverter which is working in standalone mode and is ready for synchronization to go for grid connected mode, has to closely track the grid frequency. Normally grid frequency is varying according to load variations. Any mismatch on frequency may lead to generate unwanted circulating currents and may lead to damage electronic devices. In this regard, use of PLL is widely preferred technique that enables tracking the grid frequency. PLL provides continuous information about the phase-angle and amplitude of the

magnitude of interest, generally the fundamental grid voltage, which allows space vector based controllers and modulators to be implemented, even when working with single-phase signals.

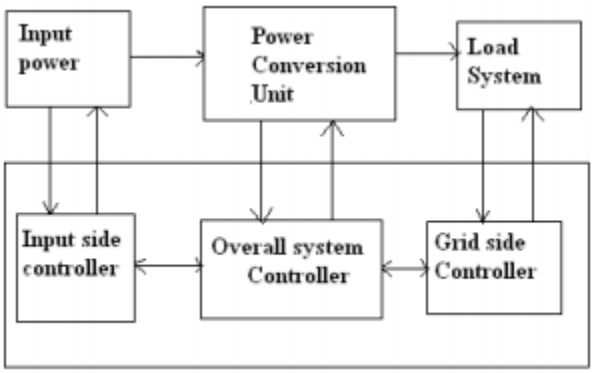


Figure 1: General structure of distributed power system

Various techniques of synchronization of the inverter based on the Phase Locked Loop (PLL) are described in the next session. Different issues and solutions related to different PLL methods are also discussed.

2 Phase Locked Loop (PLL)

The basic structure of a PLL is shown in figure 2. It consists of three fundamental blocks:

- The phase detector (PD). This block generates an output signal proportional to the phase difference between the input signal, v, and the signal generated by the internal oscillator of the PLL, v. Depending on the type of PD, high-frequency AC components appear together with the DC phase-angle difference signal.

- The loop filter (LF). This block presents a low-pass filtering characteristic to attenuate the high-frequency AC components from the PD output. Typically, this block is constituted by a first-order low-pass filter or a PI controller.

- The voltage-controlled oscillator (VCO). This block generates at its output an AC signal whose frequency is shifted with respect to a given central frequency, ω_c, as a function of the input voltage provided by the LF.

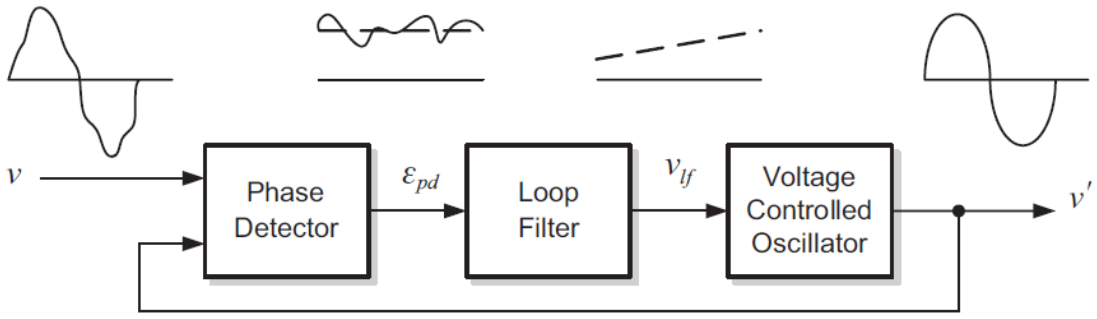


Figure 2: Basic structure of a PLL

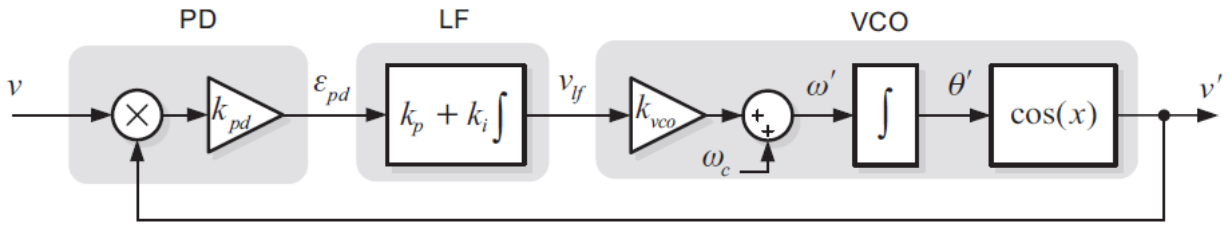


Figure 3: Block diagram of an elementary PLL

In single-phase systems there is less information than in three-phase systems regarding the grid condition, so more advanced methods should be considered in order to create an orthogonal voltage system.

The general structure of a single-phase PLL including the grid voltage monitoring is shown in figure 4. Usually, the main difference among divers single-phase PLL methods is the orthogonal voltage system generation structure.

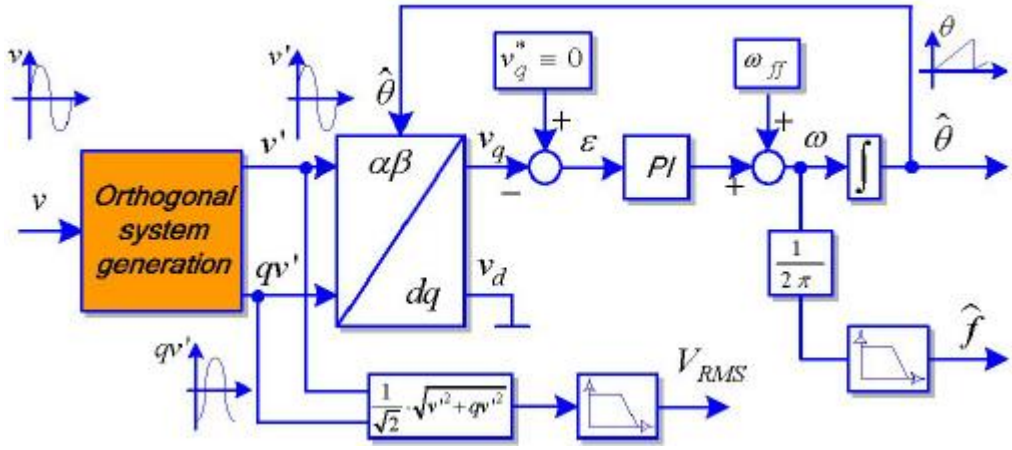


Figure 4: General structure of a single-phase PLL

An easy way of generating the orthogonal voltage system in a single-phase structure is using a transport delay block, which is responsible for introducing a phase shift of 90 degrees with respect to the fundamental frequency of the input signal (grid voltage). A related method, but more complex of creating a quadrature signal is using the Hilbert transformation. Another different method of generating the orthogonal voltage system is using an inverse Park Transformation. All this methods has some shortcomings as follows: frequency dependency, high complexity, nonlinearity, poor or none filtering. Thus, further attention should be paid on single-phase PLL systems.

In next section, single-phase PLL structure based on second order Generalized Integrator (GI) is presented. This method is a good alternative for creating an orthogonal system in single-phase systems compared to other methods.

2.1 Orthogonal system generation

This method of generating an orthogonal system is shown in figure 5. As output signals, two sine waves (v' and qv') with a phase shift of 90^0 are generated. The component v' has the same phase and magnitude as the fundamental of the input signal (v).

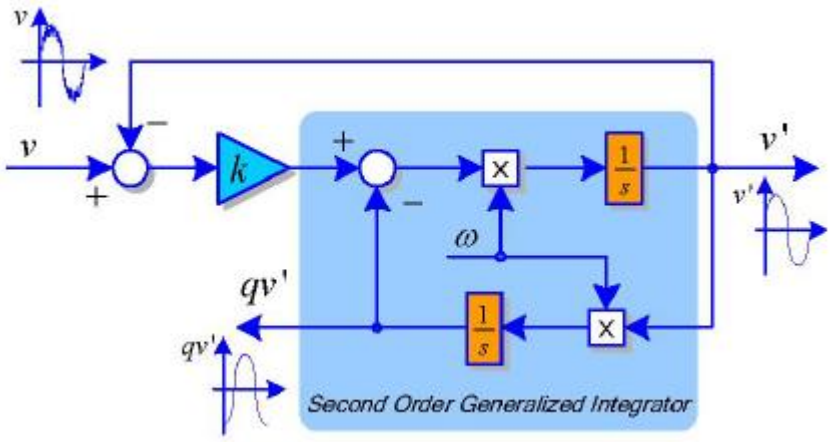


Figure 5: General structure of a single-phase PLL

Above structure is based on second order generalized integrator (SOGI):

$$GI = \frac{\omega s}{s^2 + \omega^2}$$

Where ω represents the resonance frequency of the SOGI.

The closed-loop transfer functions ($H_d = \frac{v\prime}{v}$and $H_q = \frac{qv\prime}{v}$) of the structure presented in figure 5 are defined as:

$$H_d(s) = \frac{v'}{v}(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2}$$

$$H_q(s) = \frac{qv'}{v}(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2}$$

Where k affects the bandwidth of the closed-loop system.

The PLL with SOGI was modeled in Matlab Simulink and the results are as below in figure 6:

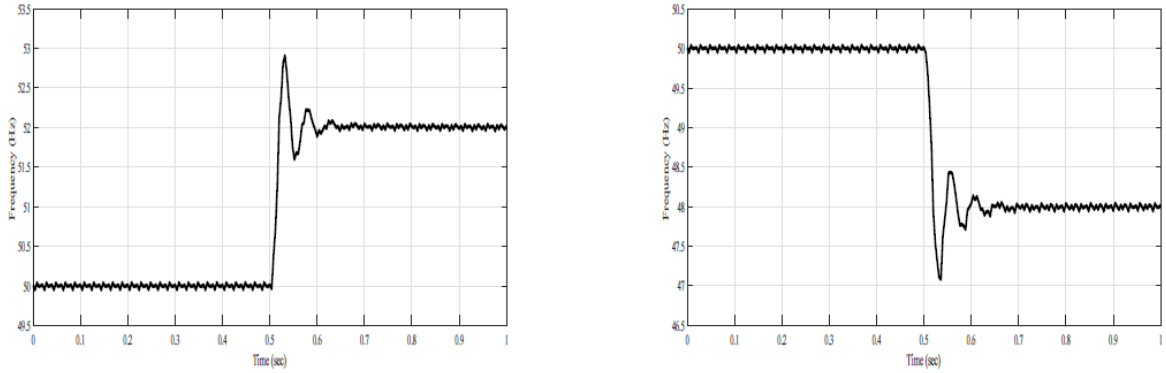
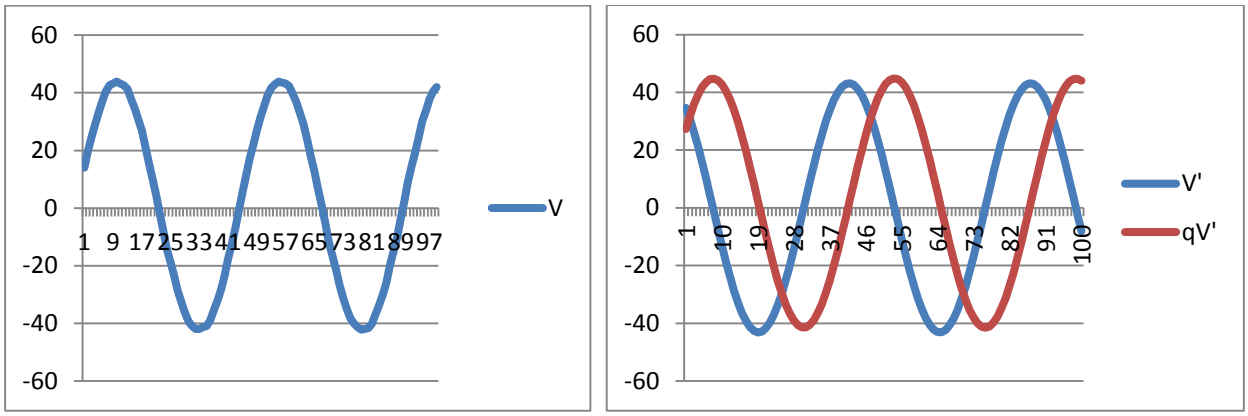


Figure 6: Result of PLL simulation in Matlab Simulink

The algorithm has been validated using sensor card and TI DSC TMS320F28335. It can be observed from figure 7(a) that a dc offset is there on the signal collected from sensor card. This offset is reflected on the output of orthogonal signal generator and frequency deviates from actual value as shown in figure 7(b).



(a) (b)

Figure 7: Hardware result for (a) input of SOGI and (b) output of SOGI

2.2 CASCADED SOGI

It is observed from the figure 7 that dc offset occurs on one of the out signal (qv') and the second signal (v') is free from dc offset. Therefore we can use v' to create orthogonal signals. In Cascaded Generalized SOGI [5] two SOGIs are connected in cascaded in which first one removes dc offset and second one creates two orthogonal signals for PLL algorithm. Figure 8 shows structure of Cascaded SOGI

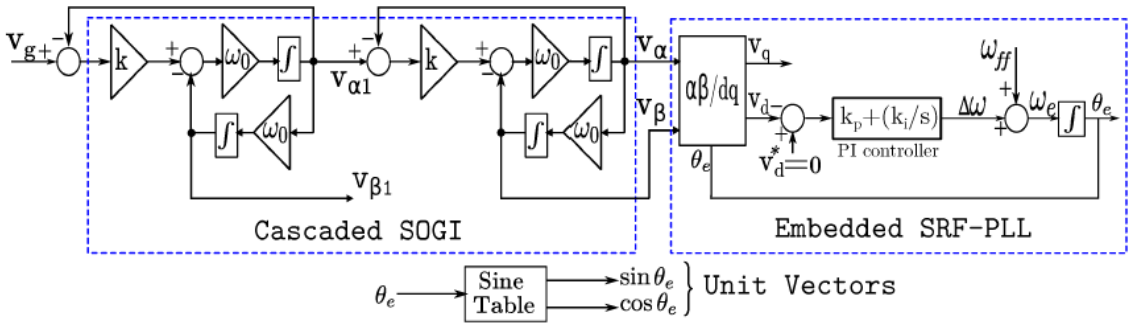
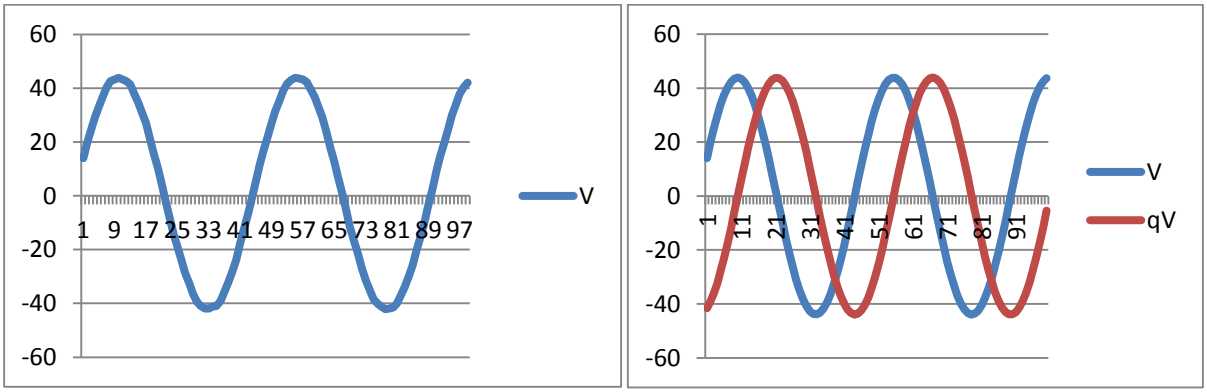


Figure 8: Structure of cascaded generalized integrator PLL (CGI-PLL)

Figure 9 presents input and output signal of cascaded generalized SOGI. From figure 9 (b), it is observed that the dc offset present in the SOGI got eliminated.



(a) (b)

Figure 9: Hardware result for (a) input of cascaded SOGI and (b) output of cascaded SOGI

Response of cascaded generalized SOGI PLL is analyzed and presented in the figure 10. It can been seen from the figure that PLL algorithm is tracking the actual frequency with a very less response time.

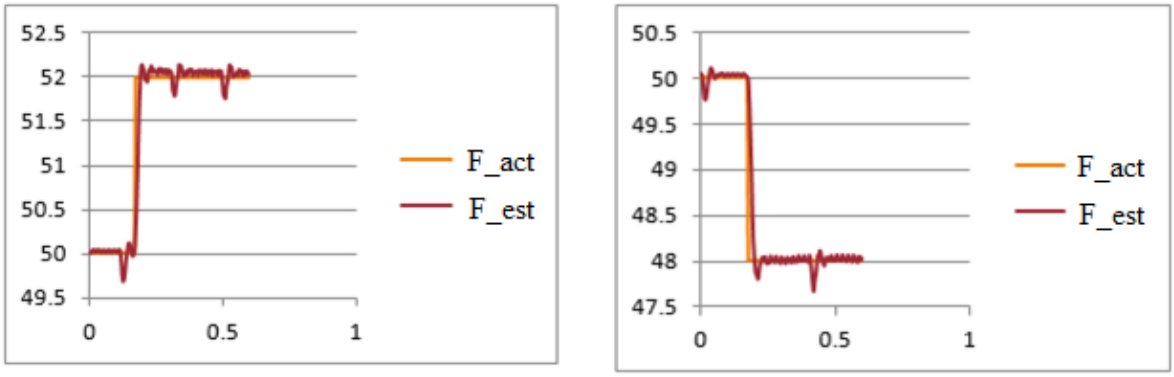


Figure 10: Hardware result of cascaded SOGI- PLL

3. RESULTS AND DISCUSSION

The study on grid synchronization algorithm is explained in this paper. The main focus was on second order generalized integrator phased locked loop which is simple and easy to implement. SOGI PLL was facing problem when a dc offset occurs on the input signal due to sensor calibration or ADC conversion issues. This problem can be eliminated using cascaded generalized SOGI. The algorithm was initially analyzed in Matlab simulink and validated in hardware.

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Author's Biodata

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